In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

A^{10} 1   1.   (Currently Amended) A data processing apparatus
2 comprising:
3   a register file comprising a plurality of registers, each of
4 said plurality of registers having a corresponding register number;
5   a first functional unit group connected to said register file
6 and including a plurality of first functional units, said first
7 functional unit group responsive to an instruction to
8   receive data from one of said plurality of registers
9   corresponding to an instruction-specified first operand
10   register number at ~~a first~~ an operand input,
11   operate   on   said   received   data   employing   an
12   instruction-specified one of said first functional units, and
13   output data to one of said plurality of registers
14   corresponding to an instruction-specified first destination
15   register number from ~~a first~~ an output;
16   a second functional unit group connected to said register file
17 and including a plurality of second functional units, said second
18 functional unit group responsive to an instruction to
19   receive data from one of said plurality of registers
20   corresponding to an instruction-specified second operand
21   register number at ~~a second~~ an operand input,
22   operate   on   said   received   data   employing   an
23   instruction-specified one of said second functional units, and
24   output data to one of said plurality of registers
25   corresponding to an instruction-specified second destination
26   register number from ~~a second~~ an output;
27   a first comparator receiving an indication of said first
28 operand register number of a current instruction and an indication
29 of said second destination register number of an immediately

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30   preceding instruction, said first comparator indicating whether
31   said first operand register number of said current instruction
32   matches said second destination register number of said immediately
33   preceding instruction; and

34   a first register file bypass multiplexer connected to said
35   register file, said first functional unit group, said second
36   functional unit group and said first comparator, said first
37   register file bypass multiplexer having a first input receiving
38   data from said register corresponding to said first operand
39   register number of said current instruction, a second input
40   connected to said ~~second~~ output of said second functional unit
41   group and an output supplying an operand to said ~~first~~ operand
42   input of said first functional unit group, said first multiplexer
43   selecting said data from said register corresponding to said first
44   operand number of said current instruction if said first comparator
45   fails to indicate a match and selecting said ~~second~~ output of said
46   second functional unit group if said first comparator indicates a
47   match;

48   said first functional units of said first functional unit
49   group and said second functional units of said second functional
50   unit group selected whereby functions often executed simultaneously
51   within the same instruction cycle have corresponding functional
52   units placed in different functional unit groups and functions
53   which are not often executed together within the same instruction
54   cycle have corresponding functional units placed in the same
55   functional unit group.

1   2.   (Currently Amended) The data processing apparatus of claim
2   1, wherein said register file, said first functional unit group,
3   said second functional unit group, said first comparator and said
4   first register file bypass multiplexer operate according to an
5   instruction pipeline comprising:

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6   a first pipeline stage consisting of a register read operation

7   from said register file to provide operands for a selected

8   functional unit of said first and second functional unit groups and

9   a first half of operation of a̶ said selected functional unit of

10   said first and said second functional unit groups, and

11   a second pipeline stage consisting of a second half of

12   operation of said selected functional unit of said first and said

13   second functional unit groups and a register write operation to

14   said register file of results of operation of said selected

15   functional unit of said first and second functional unit groups,

16   wherein the sum of the time of said register read operation

17   and said register write operation equals approximately the sum of

18   the time of said first and second halves of operation of a slowest

19   of said functional units of said first and second functional unit

20   groups.

1   3.   (Currently Amended) The data processing apparatus of claim

2   1, further comprising an output register having an input connected

3   to said s̶e̶c̶o̶n̶d̶ output of said second functional unit group and an

4   output connected to said register file for temporarily storing said

5   output of said second functional unit group prior to storing in

6   said register corresponding to said second destination register

7   number,

8   wherein said first comparator further receives an indication

9   of said second destination register number of a second preceding

10   instruction, said first comparator further indicating whether said

11   first operand register number of said current instruction matches

12   said second destination register number of said second preceding

13   instruction, and

14   wherein said multiplexer further has a third input connected

15   to said output register output, said multiplexer selecting said

16   output register output if said first comparator indicates a match.

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4.   (Canceled)

1   5.   (Currently Amended) The data processing apparatus of claim
2   1, said first comparator further receiving an indication of said
3   first destination register of said immediately preceding
4   instruction, said first comparator further indicating whether said
5   first operand register number of said current instruction matches
6   said first destination register number of said immediately
7   preceding instruction, said first multiplexer further having a
8   third input connected to said ~~first~~ output of said first functional
9   unit group, and said first multiplexer selecting said ~~first~~ output
10   of said first functional unit group if said first comparator
11   indicates a match.

1   6.   (Currently Amended) The data processing apparatus of claim
2   1, said first functional unit group further responsive to an
3   instruction to receive data from one of said plurality of registers
4   corresponding to an instruction-specified third operand register
5   number at ~~a third~~ an operand input,
6   said apparatus further comprising:
7   a second comparator receiving an indication of said third
8   operand register number of a current instruction and an indication
9   of said second destination register number of said immediately
10   preceding instruction, said second comparator indicating whether
11   said third operand register number of said current instruction
12   matches said second destination register number of said immediately
13   preceding instruction; and
14   a second register file bypass multiplexer connected to
15   said register file, said first functional unit group, said second
16   functional unit group and said second comparator, said second
17   register file bypass multiplexer having a first input receiving
18   data from said register corresponding to said third operand
19   register number of said current instruction, a second input
20   connected to said ~~second~~ output of said second functional unit

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21   group and an output supplying an operand to said ~~third~~ operand

22   input of said first functional unit group, said second multiplexer

23   selecting said data from said register corresponding to said third

24   operand number of said current instruction if said second

25   comparator fails to indicate a match and selecting said ~~second~~

26   output of said second functional unit group if said second

27   comparator indicates a match.

1   7.   (Currently Amended) The data processing apparatus of claim

2   6, said first comparator further receiving an indication of said

3   first destination register of said immediately preceding

4   instruction, said first comparator further indicating whether said

5   first operand register number of said current instruction matches

6   said first destination register number of said immediately

7   preceding instruction, said first multiplexer further having a

8   third input connected to said ~~first~~ output of said first functional

9   unit group, said first multiplexer selecting said ~~first~~ output of

10   said first functional unit group if said first comparator indicates

11   a match,

12   said second comparator further receiving an indication of said

13   first destination register of said immediately preceding

14   instruction, said second comparator further indicating whether said

15   third operand register number of said current instruction matches

16   said first destination register number of said immediately

17   preceding instruction, said second multiplexer further having a

18   third input connected to said ~~first~~ output of said first functional

19   unit group, and said second multiplexer selecting said ~~first~~ output

20   of said first functional unit group if said second comparator

21   indicates a match.

1   8.   (Currently Amended) The data processing apparatus of claim

2   1 further comprising:

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3   a ~~third~~ second comparator receiving an indication of said
4   second operand register number of a current instruction and an
5   indication of said second destination register number of an
6   immediately preceding instruction, said ~~third~~ second comparator
7   indicating whether said second operand register number of said
8   current instruction matches said second destination register number
9   of said immediately preceding instruction; and

10   a ~~third~~ second register file bypass multiplexer connected to
11 said register file, said first functional unit group, said second
12 functional unit group and said ~~third~~ second comparator, said second
13 register file bypass multiplexer having a first input receiving
14 data from said register corresponding to said second operand
15 register number of said current instruction, a second input
16 connected to said ~~second~~ output of said second functional unit
17 group and an output supplying an operand to said ~~second~~ operand
18 input of said second functional unit group, said ~~third~~ second
19 multiplexer selecting said data from said register corresponding to
20 said second operand number of said current instruction if said
21 ~~third~~ second comparator fails to indicate a match and selecting
22 said ~~second~~ output of said second functional unit group if said
23 ~~third~~ second comparator indicates a match.

1   9.   (Currently Amended) The data processing apparatus of claim
2   8, said ~~third~~ second comparator further receiving an indication of
3   said first destination register number of an immediately preceding
4   instruction, said ~~third~~ second comparator indicating whether said
5   second operand register number of said current instruction matches
6   said first destination register number of said immediately
7   preceding instruction, said ~~third~~ second multiplexer further having
8   a third input connected to said ~~first~~ output of said first
9   functional unit group, and said ~~third~~ second multiplexer further
10 selecting said ~~first~~ output of said first functional unit group if
11 said ~~third~~ second comparator indicates a match.

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A10   12   10.   (Canceled)

1   11.   (Currently Amended)   A   data   processing   apparatus
2   comprising:
3   a first register file comprising a plurality of registers,
4   each of said plurality of registers having a corresponding register
5   number;
6   a second register file comprising a plurality of registers,
7   each of said plurality of registers having a corresponding register
8   number;
9   a first functional unit group including an input connected to
10   said first and second register files, an output connected to said
11   first register file, and a plurality of first functional units, said
12   first functional unit group responsive to an instruction to
13   receive data from one of said plurality of registers in
14   said first and second register files corresponding to an
15   instruction-specified first operand register number at ~~a first~~
16   an operand input,
17   operate   on   said   received   data   employing   an
18   instruction-specified one of said first functional units, and
19   output data to one of said plurality of registers in said
20   first register file corresponding to an instruction-specified
21   first destination register number from ~~a first~~ an output;
22   a second functional unit group including an input connected to
23   said first and second register files, an output connected to said
24   second register file, and a plurality of second functional units,
25   said second functional unit group responsive to an instruction to
26   receive data from one of said plurality of registers in
27   said first and second register files corresponding to an
28   instruction-specified second operand register number at ~~a~~
29   ~~second~~ an operand input,

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30   operate on said received data employing an
31   instruction-specified one of said second functional units, and
32   output data to one of said plurality of registers in said
33   second register file corresponding to an instruction-specified
34   second destination register number from ~~a second~~ an output;
35   and
36   a first crosspath connecting said second register file to said
37   first functional unit group comprising
38   a first crosspath comparator, wherein, if said first
39   operand register is in said second register file, said
40   comparator receives an indication of said first operand
41   register number of a current instruction and an indication of
42   said second destination register number of a preceding
43   instruction, and said first crosspath comparator indicates
44   whether said first operand register number of said current
45   instruction matches said second destination register number of
46   said preceding instruction, and
47   a first crosspath multiplexer connected to said second
48   register file, said first functional unit group, said second
49   functional unit group and said first crosspath comparator,
50   <u>said first crosspath multiplexer</u> having a first input
51   receiving data from said register corresponding to said first
52   operand register number of said current instruction, a second
53   input connected to said ~~second~~ output of said second
54   functional unit group and an output supplying an operand to
55   said ~~first~~ operand input of said first functional unit group,
56   wherein, if said first operand register is in said second
57   register file, said first crosspath multiplexer selects said
58   data from said register corresponding to said first operand
59   number of said current instruction if said first crosspath
60   comparator fails to indicate a match and selects said ~~second~~

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61 output of said second functional unit group if said first
62 crosspath comparator indicates a match;
63 said first functional units of said first functional unit
64 group and said second functional units of said second functional
65 unit group selected whereby functions often executed simultaneously
66 within the same instruction cycle have corresponding functional
67 units placed in different functional unit groups and functions
68 which are not often executed together within the same instruction
69 cycle have corresponding functional units placed in the same
70 functional unit group.

12 to 16. (Canceled)

1 17. (New) The data processing apparatus of claim 1, wherein:
2 said first functional unit group wherein
3   each first functional unit includes a output, and
4   further including an output multiplexer having a
5 plurality of inputs receiving respective outputs of said first
6 functional units and an output, said output multiplexer
7 selecting said output of said instruction-selected one of said
8 first functional units; and
9 said second functional unit group wherein
10   each second functional unit includes a output, and
11   further including an output multiplexer having a
12 plurality of inputs receiving respective outputs of said
13 second functional units and an output, said output multiplexer
14 selecting said output of said instruction-selected one of said
15 second functional units.

1 18. (New) The data processing apparatus of claim 2, wherein:
2 each first functional unit of said first functional unit group
3 and each second functional unit of said second functional unit

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4   group includes a pipeline latch in the middle for latching a
5   logical state of said functional unit between said first pipeline
6   stage and said second pipeline stage.

1   19.   (New) The data processing apparatus of claim 11, wherein:
2   said first functional unit group wherein
3   each first functional unit includes a output, and
4   further including an output multiplexer having a
5   plurality of inputs receiving respective outputs of said first
6   functional units and an output, said output multiplexer
7   selecting said output of said instruction-selected one of said
8   first functional units; and
9   said second functional unit group wherein
10   each second functional unit includes a output, and
11   further including an output multiplexer having a
12   plurality of inputs receiving respective outputs of said
13   second functional units and an output, said output multiplexer
14   selecting said output of said instruction-selected one of said
15   second functional units.

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